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TO: Exr. A. Kinkead, Art Unit 2817
COMPANY: U.S. PATENT & TRADEMARK OFFICE
FAX: 703-872-9318
FROM: Steven Lin, Reg. No. 35,250
DATE: February 23, 2004
SUBJECT: USSN 10/612,200

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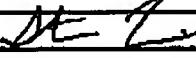
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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>		Application Number 10/612,200
		Filing Date 7/3/2003
		First Named Inventor MAXIM
		Art Unit 2817 (prior)
		Examiner Name Arnold Kinkead (prior)
Total Number of Pages in This Submission 3		Attorney Docket Number 1083-MS-C1

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PTO/SB/08A (04-03)

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 11 of 2

of 2

Complete If Known

Application Number	10/612,200
Filing Date	7/3/2003
First Named Inventor	MAXIM
Art Unit	2817 (prior)
Examiner Name	Arnold Kinhead (prior)
Attorney Docket Number	1083-MS-C1

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner Signature		Date Considered	
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	10/612,200
		Filing Date	7/3/2003
		First Named Inventor	MAXIM
		Art Unit	2817 (prior)
		Examiner Name	Arnold Kinkead (prior)
Sheet	2	of	2
		Attorney Docket Number	
		1083-MS-C1	

NON-PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
	2	YOUNG et al., A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," J. Solid-State Circuits, 27(11):1599-1607, Nov. 1992.		
	3	MANEATIS, J.G., "Low-Jitter Process-Independent DLL and PLL Base on Self-Biased Techniques," J. Solid-State Circuits, 31(11):1723-1732, Nov. 1996		
	4	MIJUSKOVIC et al., "Cell-Based Fully Integrated CMOS Frequency Synthesizers," J. Solid-State Circuits, 29(3):271-279, Mar. 1994		
	5	NOVOF et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter," J. Solid-State Circuits, 30(11):12592-12696, Nov. 1995.		
	6	LEE and KIM, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," J. Solid-State Circuits, 35(8):1137-1145, Aug. 2000.		
	7	LIN et al., "A 1.4GHz Differential Low-Noise CMOS Frequency Synthesizer Using a Wideband PLL Architecture," ISSCC Dig. Tech. Papers, San Francisco, CA, Feb. 2000, pp. 147-149		
	8	RHEE, W., "Design of High Performance CMOS Charge-Pumps in Phase-Locked Loops," Proc. IEEE Int. Symp. Circuits and Systems, Orlando, FL, May 1999, pp. II-545-II-548.		
	9	MAXIM et al., "A Low Jitter 125-1250 MHz Process Independent 0.18µm CMOS PLL Based on a Sample-Reset Loop Filter," ISSCC Dig. Tech. Papers, San Francisco, CA, Feb. 2001, pp. 394-395		
	10	MAXIM & MAXIM, "A Novel Physical Model of Deep-Submicron CMOS Transistors Mismatch for Monte Carlo SPICE Simulation," Proc. IEEE Int. Symp. Circuits and Systems, Sydney, NSW, Australia, May 2001, pp. V.511-V.514.		

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